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Two op amps make fast full-wave rectifier

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The circuit in **Figure 1** is a precision full-wave rectifier with the following characteristics:

- Minimal delay time between the input and output (with only one op amp in the chain);
- Similar delay times for positive and negative inputs;
- No need to match diodes or adjust resistors.

When $V_{IN}>0V$, the output of op amp IC_1 is negative, so the reverse-biased diode D_1 blocks the output path of IC_1 to V_{OUT}. The output of op amp IC_2 is positive, so the forward-biased diode D_2 sets the voltage V_B at $V_{IN}(R_6/(R_6+R_5))$. The gain of this noninverting amplifier is $(R_6/(R_6+R_5))(1+R_3/R_4)$.

When $V_{IN}<0V$, the output of op amp IC_1 is positive, so $V_A=0V$, diode D_1 becomes forward-biased, and the gain of the inverting amplifier is R_2/R_1. The output of op amp IC_2 is negative, so the reverse-biased diode D_2 blocks the output path of IC_2 to V_{OUT}. Three cases are possible for the circuit in **Figure 1**:

- For unity gain, $R_3=R_5=0\Omega$, $R_4=R_6=\infty$, and $R_1=R_2$. For the project that led to this design, $R_1=R_2=4.75k\pm1\%$, and the input is a sine wave at 25 Hz and 4V rms.
- For gains greater than unity, $R_5=0\Omega$, $R_6=\infty$, and the gain is $R_2/R_1=(1+R_3/R_4)$. Satisfying this gain equation yields equal gains for positive and negative input signals.
- For gains lower than unity, $R_3=0\Omega$, $R_4=\infty$, and the gain is $R_2/R_1=R_6/(R_6+R_5)$. Satisfying this gain equation yields equal gains for positive and negative input signals. (DI #1837) EDN

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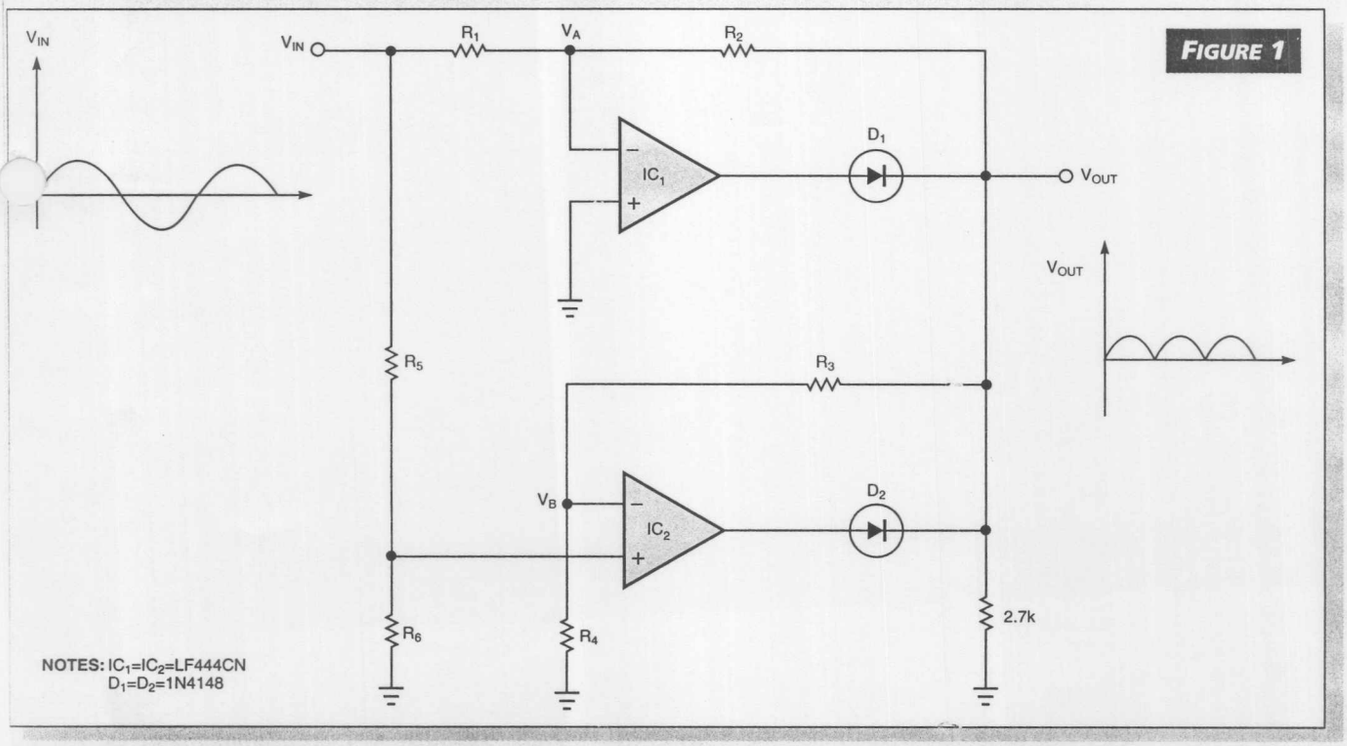

You can obtain precision full-wave rectification with any desired gain, with no need to match diodes or trim resistors.

Network forms digital-to-impedance converter

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The circuit in **Figure 1** resembles a capacitive-ladder (C-2C) D/A converter. However, it does not provide conversion from a digital code to a voltage or current, but rather converts the digital code to a capacitor value. The C-2C topology is well-suited for IC or hybrid implementation, as it calls for only two nominal values. You can prove mathematically that the equivalent capacitance between terminals 1 and 2 is $C_{EQ}=2C\cdot(D_i\cdot2^{-i})$, where D_i represents the binary coefficients of the digital-input code.

The follower IC_1 keeps both buses I_1 and I_2 at equal poten-